*International Journal of scientific research and management (IJSRM)*
*||Volume|| 1 ||Issue|| 4 ||Pages|| 238-240||2013||*
*Website: www.ijsrm.in ISSN (e): 2321-3418*

# Sopc based convolutinal Encoder and Viterbi Decoder

***Tejasweeni G. Bhangale, Prof. K.S.Bhagat***
*M.E.II(EXTC) J. T.Mahajan College of Engineering,Faizpur.*
*Asst.Professor J. T.Mahajan College of Engineering,Faizpur.*
tejuu55@rediffmail.com
ksbhagat@rediffmail.com

***Abstract*— Convolutional encoding is most important technique in Code Division Multiple Acess(CDMA).CDMA uses convolutional encoder to reduce interference. Convolutional encodeing and viterbi decoding are most widely used in most communication systems because of their excellant error control. Convolutional encoding with Viterbi decoding is a FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by additive white gaussian noise (AWGN). The design has been implemented on SOPC using XILINX 12.2 software with supporting simulation tool ISim.**

***Keywords*—Convolutional encoder, Viterbi decoder,VHDL, Isim simulator, FPGA**

## I. INTRODUCTION

SOPC is nothing but system on programming chip. It is semiconductor device containing programmable logic components and interconnects. The programmable logic components can be programmed to implement the function of basic logic gates such as AND, OR, NOT, XOR or more complex combinational functions such as encoder and decoder or simple math functions. These programmable logic devices also include memory elements, which may be simple flip-flops or more complex blocks of memories [5] . In order to design the behavior of the SOPC, users must provide a Hardware Description Language [HDL].Such as Verilog Hardware Description Language or VHDL

Due to weaknesses of using the block codes for error correction in useful channels, another approach of coding called convolutional coding had been introduced in 1955 [1]. Convolutional encoding and the viterbi decoding both are the least error techniques. So here we tried to reduce the errors by using same technique with the implementation of FPGA.

.

## II. ENCODER HARDWARE DESIGN

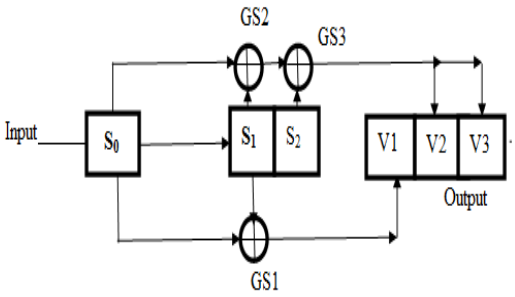



Figure 1. Convolutional Encoder

. A Convolutional encoder can be viewed as a finite state machine. It can be implemented with registers ,XOR gates and a multiplexer .A Convolutional coding is done by combining the fixed number of input bits .The Input bits are stored in the fixed length shift register and they are combined with the help of mod-2 adders. This operation is equivalent to binary convolution and hence it is called Convolutional coding.

From Figure 1. it is observed that whenever the message bit is shifted to position S0, the new values of V1, V2 and V3 are generated depending upon S0, S1, and S2. To represent the output of previous two message bits S1 and S2 are used. The current bit is present in S0. Output of the convolution encoder is,

V1 = S0 **XOR (GS1)** S1 ---------- (1)
V2= S0 **XOR (GS2)**S1 **XOR (GS3)** S2 --------- (2)
V3= S0 **XOR (GS2)**S1 **XOR (GS3)** S2---------- (3)

The convolutional encoder operates by passing the input bit in S0 and shift to S0-S1-S2 in one operation and accordingly output bit V1, V2 & V3 varies. Table 2.1 shows detailed step wise operation for variation in state of the encoder.

It can be implemented by using following procedure:

1. Generate 1MHz clock from the clock division.
2. Give start signal for encoding.
3. Take the input data in the form of 7, 8 and 9 bits.

4. Do the Convolution encoding with respective code rate.

5. After encoding transmit the data serially

## III. DECODER HARDWARE DESIGN

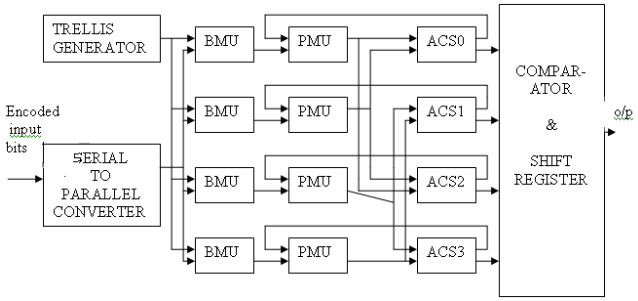



Fig.2 Viterbi Decoder

Decoder decodes the message [2]. For encoding the convolutional encoding which is most efficient technique in digital communication systems[3]. A viterbi decoder drops the least likely trellis path at each transmission stage. In this way, it decreases decoding complexity with early rejection of unlike paths and gets its efficiency via concentrating on survival paths of the trellis. The receiver receives the serial encoded data and converts it into 3 bit parallel data.

Fig 2 shows a typical viterbi decoder. It has BMU(nranch metric unit),PMU(path metric unit) and ACS(add and compare unit). A viterbi decoder drops the least likely trellis path at each transmission stage usig all available paths through Trellis with ACS. In this way, it decreases decoding complexity with early rejection of unlike paths and gets its efficiency via concentrating on survival paths of the trellis.

It follows following procedure:

1. Wait for falling edge to be detected, after detecting falling edge sample after 52µsec.
2. Now sample the next bits.
3. after all bits are received check that next bit received is STOP bit.
4. Give the received data to the Viterbi decoder for decoding.
5. After decoding output the data which is original information transmitted.

## IV. SIMULATION USING FPGA

FPGA is nothing but system on programming chip. It is semiconductor device containing programmable logic components and interconnects. VHDL is commonly used as a design-entry language for FPGA and application-specific integrated circuits in electronic design automation of digital circuits. VHDL comes from VHSIC hardware description language, where VHSIC stands for very high- speed integrated circuit. The process starts with Register Transfer Level (RTL) coding which comprises of Behavioral description and Hardware Description Language (HDL).

## V RESULTS AND DISCUSSION

| Bit Length | Code Rate | Number of Errors | Bit Error rate |
|---|---|---|---|
| 7 | ½ | 2 | 28.57 % |
| | 1/3 | 3 | 42.85 % |
| 8 | ½ | 1 | 12.5 % |
| | 1/3 | 3 | 37.5% |
| 9 | ½ | 2 | 22.22% |
| | 1/3 | 4 | 44.44% |

Fig. 3. Comparison Table

The output for the encoder and decoder is shown in fig.4 and 5.

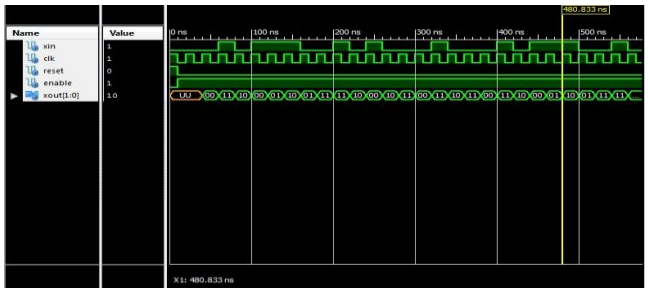
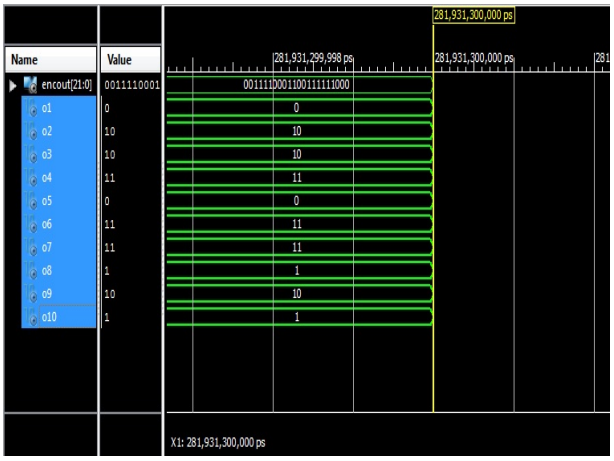


Fig.4 Encoder output

Fig 5 Decoder output



## V. CONCLUSION

It is observed from the table that with increase in code rate and constraint length bit error rate is also increased. Hence we

conclude that viterbi decoding is limited to lower constraint length.

Future work is focused on design of convolutional encoder and viterbi decoder with more than 9-bit constraint length.


## ACKNOWLEDGMENT

Authers would like to thank IIEEE and IJETEE board that they had provided us an opportunity to publish our paper in their journal. We are looking forward for suggestions from board about our work.


## REFERENCES


[1] I. Kang, A. N. W. Jr, "*Low-Power Viterbi Decoder for CDMA Mobile Terminals*", IEEE J. Solid-State Circuits, vol. 33, no. 3, Mar. 1998.

[2] B. W. Kim, J. H. Yang, C. M. Kyung, et al., "*MDSP: 16-bit DSP with Mobile Communication Accelerator*", in Proc. IEEE Custom Integrated Circuits
Conference, pp. 2.1.1-2.1.4, 1998.

[3] Tuominen J. and Plosila J ., "*Asynchronous Viterbi Decoder in Action Systems*", TUCS Technical Report, No. 710, September 2005.

[4] Lin C. C., Shih Y. H., Chang H. C., and Lee C. Y.." *A Low Power Turbo/ Viterbi Decoder for 3GPP2 Applications*", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 4, pp. 426-430, April 2006.

[5] Lin Y. Baron N., Lee Y, Mahlke S., and Mudge T., "*A Programmable Vector Coprocessor Architecture for Wireless Applications*", Advanced computer architecture
laboratory, University of Michigan, 2004.
http://www.eecs.umich.edu~tnmpaperswasp04.pdf

[6] Ken Chapman, "*NOR FLASH Programmer for Spartan-3E Starter Kit*", User Guide , Xilinx Ltd., March 2006. Available Via Internet at Web Site:
http://www.xilinx.com/products/boards/s3estarter/
files/s3esk_picoblaze_nor_flash_programmer.pdf

[7] Jameel Hussein, "*Multiple-Boot with Platform Flash PROMs*", Application Note on
Spartan-3E FPGA, Xilinx Company, April 2007. Available Via Internet at Web Site:
http://www.xilinx.com/support/documentation/application_notes/xapp483.pdf

[8] B. Sklar, "*Digital Communications Fundamentals and Applications*", Prentice Hall, Second Edition, 2001.